

What is claimed is:

1 1. ~~An SRAM memory cell comprising:~~

2 first and second transfer gate transistors, the first
3 transfer gate transistor having a first source/drain
4 connected to a bit line and the second transfer gate
5 transistor having a first source/drain connected to a
6 complement bit line and each transfer gate transistor
7 having a gate connected to a word line; and

8 first and second pull-down transistors configured as
9 a storage latch, the first pull-down transistor having a
10 first source/drain connected to a second source/drain of
11 said first transfer gate transistor and the second pull-
12 down transistor having a first source/drain connected to a
13 second source/drain of said second transfer gate
14 transistor, both first and second pull-down transistors
15 having a second source/drain connected to a power supply
16 voltage node;

17 wherein the first and second transfer gate transistors
18 each include a gate oxide layer having a first thickness,
19 the first and second pull-down transistors each include a
20 gate oxide layer having a second thickness, and the first
21 thickness is different from the second thickness.

1 2. The SRAM memory cell of claim 1, wherein the first
2 thickness is thicker than the second thickness.

1 3. The SRAM memory cell of claim 2, wherein the first
2 thickness is greater than two times the second thickness.

1 4. The SRAM memory cell of claim 1, wherein the first and
2 second thicknesses are determined as follows:

TI 30 X

$$RATIO \leq \frac{TOX_{tg}}{TOX_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{VCC - Vt_{tg}}{VCC - Vt_{pd}}$$

4 where RATIO is the desired ratio of the transfer gate
5 transistors and the pull-down transistors, TOx_{tg} is the gate
6 oxide thickness of the transfer gate transistor, TOx_{pd} is
7 the gate oxide thickness of the pull-down transistor, W_{pd} is
8 width of the pull-down transistor, L_{pd} is the length of the
9 pull-down transistor, W_{tg} is the width of the transfer gate
10 transistor, L_{tg} is the length of the transfer gate
11 transistor, Vt_{tg} is the threshold voltage of the transfer
12 gate transistor, and Vt_{pd} is the threshold voltage of the
13 pull-down transistor.

1 5. The SRAM memory cell of claim 4, wherein RATIO is
2 equal to 2.6.

1 6. A method for fabricating two transistors in a
2 semiconductor device comprising:

3 forming a first transistor having a first gate
4 including a gate oxide layer having a first thickness; and

5 forming a second transistor having a second gate
6 including a gate oxide layer having a second thickness,
7 wherein the second thickness is greater than the first
8 thickness.

1 7. The method of claim 6, wherein said step of forming a
2 second transistor comprises:

3 forming a gate oxide over a substrate in a region of
4 the second transistor when the first gate is formed,
5 wherein the gate oxide layer in region of the second
6 transistor initially has a first thickness;

7 thereafter, depositing a protective layer over the
8 semiconductor device;

9 opening a window in the protective layer over the
10 region of the second transistor;

11 etching away the gate oxide in the window to expose
12 the substrate; and

13. A semiconductor circuit comprising:

2 a first transistor having a first gate including a
3 gate oxide layer having a first thickness; and

4 a second transistor having a second gate including a
5 gate oxide layer having a second thickness, wherein the
6 second thickness is greater than the first thickness.

7 14. The semiconductor circuit of claim 13, wherein the
1 first transistor is a pull-down transistor in an SRAM
2 memory cell.

8 15. The semiconductor circuit of claim 14, wherein the
1 second transistor is a transfer gate transistor in the SRAM
2 memory cell.

9 16. The semiconductor circuit of claim 15, wherein the
1 gate oxide thickness of the pull-down transistor and a
2 transfer gate transistor in the SRAM memory cell are
3 selected using the following:

10
$$RATIO \leq \frac{TOX_{tg}}{TOX_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{VCC-Vt_{tg}}{VCC-Vt_{pd}}$$

11 where RATIO is the desired ratio of the transfer gate
12 transistors and the pull-down transistors, TOX_{tg} is the gate
13 oxide thickness of the transfer gate transistor, TOX_{pd} is
14 the gate oxide thickness of the pull-down transistor, W_{pd} is
15 width of the pull-down transistor, L_{pd} is the length of the
pull-down transistor, W_{tg} is the width of the transfer gate
transistor, L_{tg} is the length of the transfer gate
transistor, Vt_{tg} is the threshold voltage of the transfer
gate transistor, and Vt_{pd} is the threshold voltage of the
pull-down transistor.

16 17. The semiconductor circuit of claim 16, wherein RATIO
1 is at least 2.6.

1 11 18. The semiconductor circuit of claim 21, wherein the
2 pull-down transistor is an n-channel field effect devices.

1 12 19. The semiconductor circuit of claim 18, wherein the
2 transfer gate transistor is an n-channel field effect
3 device.

13 forming a gate oxide on the exposed substrate until a
14 gate oxide layer of the second thickness is reached.

1 8. The method of claim 7, wherein said step of forming a
2 second transistor comprises:

3 forming a gate oxide layer over a substrate in a
4 region of the second transistor when the first gate is
5 formed, wherein the gate oxide layer in the second gate has
6 a thickness equal to the first thickness; and

7 forming additional gate oxide on the gate oxide layer
8 in the region of the second transistor until the gate oxide
9 layer in the region of the second transistor reaches the
10 second thickness.

1 9. The method of claim 4, wherein the step of forming a
2 first transistor comprises forming a pull-down transistor
3 in an SRAM memory cell.

1 10. The method of claim 9, wherein the step of forming a
2 second transistor comprises forming a transfer gate
3 transistor in the SRAM memory cell.

1 11. The method of claim 10, wherein the steps of forming
2 a pull-down transistor and a transfer gate transistor in
3 the SRAM memory cell comprises forming the transistors to
4 achieve a resistivity ratio as follows:

$$5 \text{ RATIO} \leq \frac{\text{TOX}_{tg}}{\text{TOX}_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{VCC-Vt_{tg}}{VCC-Vt_{pd}}$$

6 where RATIO is the desired ratio of the transfer gate
7 transistors and the pull-down transistors, TOX_{tg} is the gate
8 oxide thickness of the transfer gate transistor, TOX_{pd} is
9 the gate oxide thickness of the pull-down transistor, W_{pd} is
10 width of the pull-down transistor, L_{pd} is the length of the
11 pull-down transistor, W_{tg} is the width of the transfer gate
12 transistor, L_{tg} is the length of the transfer gate
13 transistor, Vt_{tg} is the threshold voltage of the transfer

14 gate transistor, and $V_{t_{pd}}$ is the threshold voltage of the
15 pull-down transistor.

1 12. The method of claim 11, wherein the step of forming
2 the transistors includes using a RATIO equal to at least
3 2.6.